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Substitution for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
Application Number				10/046,937	
Filing Date				01/14/02	
First Named Inventor				Jeff C. KLEIN et al.	
Art Unit				2819	
Examiner Name				Unknown	
Attorney Docket Number				H0002065	
Sheet	2	of	2		

[illegible]

Examiner Signature	<i>[Signature]</i>	Date Considered	10/14/2001
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*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

'Applicant's unique citation designation number (optional). 'Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	10/048,937
				Filing Date	01/14/02
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				Examiner Name	Unknown
Sheet	1	of	2	Attorney Docket Number	H0002065

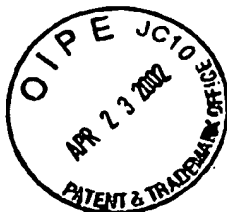
U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
		US-6,021,271	02/01/2000	Winter et al.	
		US-6,272,451 B1	08/07/2001	Mason et al.	
		US-			
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FOREIGN PATENT DOCUMENTS						
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		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
		EP 0 485 199 A2	13.05.92	Matra Design Semiconductor, Inc.		

Examiner Signature		Date Considered	10/14/2004
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PTO/SB/08B (10-01)

Approved for use through 10/31/2002. OMB 0651-0031

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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/046,937
		Filing Date	January 14, 2002
		First Named Inventor	Jeff C. Klein
		Group Art Artist	
		Examiner Name	
Sheet	2 of 2	Attorney Docket Number	H0002065

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Implementation Technology, Chapter 3, April 5, 1999, Pages 61-100.	
		XESS CORPORATION, "What are CPLDs and FPGAs?", http://www.xess.com/fpgatut.htm , Date visited: 3/20/02, 3 pages.	
		RICHARD GEISLER, "1.2.1 Basics of Synthesis and Optimization", http://mikro.e-technik.uni-ulm.de/vhdl/anl-engl.syn/html/node10.html , Date visited: 3/20/02, 2 pages.	
		RICHARD GEISLER, "1.2.2 Logic-Level Optimization", http://mikro.e-technik.uni-ulm.de/vhdl/anl-engl.syn/html/node11.html , Date visited: 3/20/02, 3 pages.	
		RICHARD GEISLER, "1.3 Synthesis Design Flow", http://mikro.e-technik.uni-ulm.de/vhdl/anl-engl.syn/html/node12.html , Date visited: 3/20/02, 3 pages.	
		Language Overview, "What is VHDL", www.acc-eda.com/vhdlref/refguide/language_overview/language_overview.htm , Date visited: 12/26/01, 3 pages.	
		Language Overview, "Test Benches", www.acc-eda.com/vhdlref/refguide/language_overview/test_benches/test_benches.htm , Date visited: 12/26/01, 11 pages.	

Examiner Signature		Date Considered	10/14/2002
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